EEL 4744

EEL 4744C: µP Apps

Menu

- More on Timer-Counter, this time with **INTERRUPTS** for output timing

See docs/examples on web-site:
`doc8331 (Sec 14), doc8385 (Sec 16)`

1

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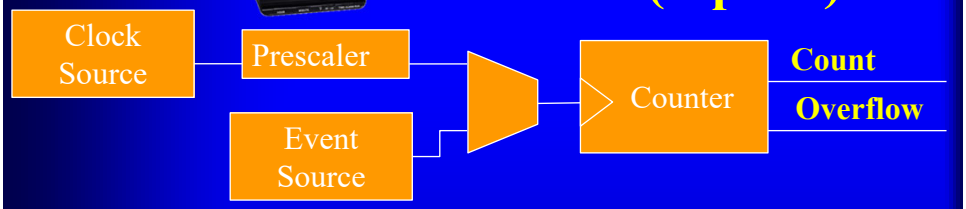
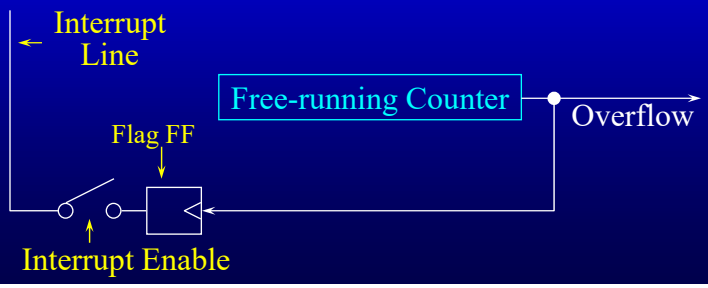
Timer/Counter and Overflow (reprise)



- An overflow occurs when the counter rolls over from the maximum (or some other value) to 0



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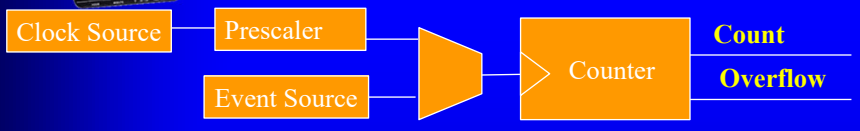
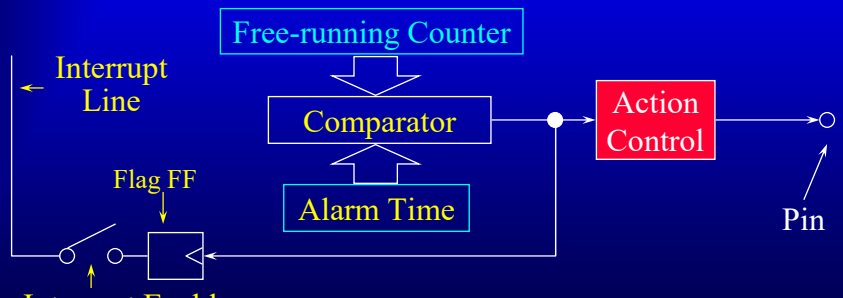
Timer/Counter Alarms (Output Compare) (reprise)



- An "alarm" will occur when the count matches a specified **alarm time**



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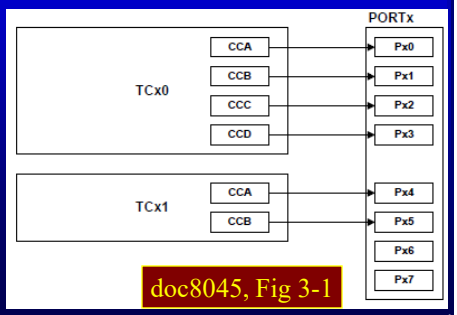
XMEGA CCx (reprise)

- Timer TCxn, where x indicates the port (C, D, E, or F) and n is the TC number within PORTx.
  - >Example: TCD0 is Timer/Counter 0 connected to PORTD
  - >The compare or capture channels consist of a set of 16-bit registers named CCx[H:L].
  - >Timer0, with 4 channels, has
    - CCA[H:L], CCB[H:L], CCC[H:L], and CCD[H:L]
  - >Timer1, with 2 channels has
    - CCA[H:L] and CCB[H:L]



See doc8045, Sec 3.1

See doc8045, Sec 3-5

doc8045, Fig 3-1

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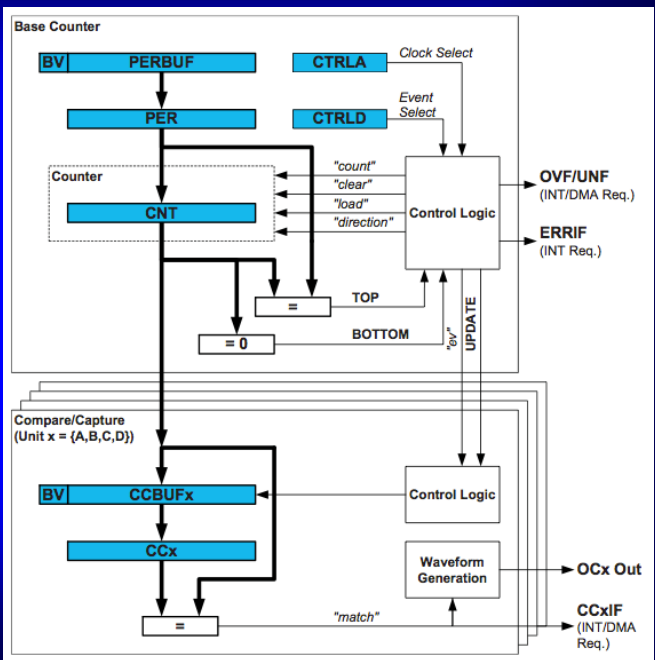
XMEGA Timer System Block Diagram



doc8331: Figure 14-2

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EEL 4744

XMEGA Single-slope Pulse Width Modulation (PWM)

- Both the Overflow Status Flag (OVFIF) and the multiple Compare Flags (CCxIF) may be used to generate interrupts
- When enabled, these interrupts may be used to update the period and compare buffer values

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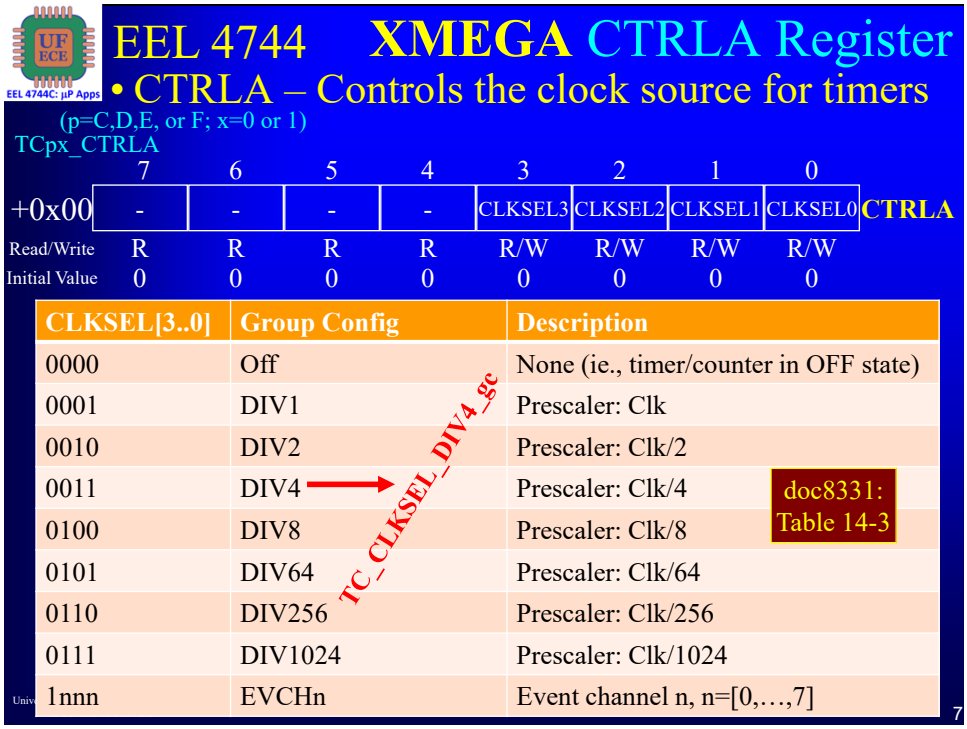
EEL 4744 XMEGA CTRLA Register
• CTRLA – Controls the clock source for timers
(p=C,D,E, or F; x=0 or 1)
TCpx_CTRLA
7 6 5 4 3 2 1 0
+0x00 - - - - CLKSEL3 CLKSEL2 CLKSEL1 CLKSEL0 CTRLA
Read/Write R R R R R/W R/W R/W R/W
Initial Value 0 0 0 0 0 0 0 0
CLKSEL[3..0] | Group Config | Description
0000 | Off | None (ie., timer/counter in OFF state)
0001 | DIV1 | Prescaler: Clk
0010 | DIV2 | Prescaler: Clk/2
0011 | DIV4 | Prescaler: Clk/4
0100 | DIV8 | Prescaler: Clk/8
0101 | DIV64 | Prescaler: Clk/64
0110 | DIV256 | Prescaler: Clk/256
0111 | DIV1024 | Prescaler: Clk/1024
1nnn | EVCHn | Event channel n, n=[0,…,7]
TC_CLKSEL_DIV4_gc
doc8331: Table 14-3
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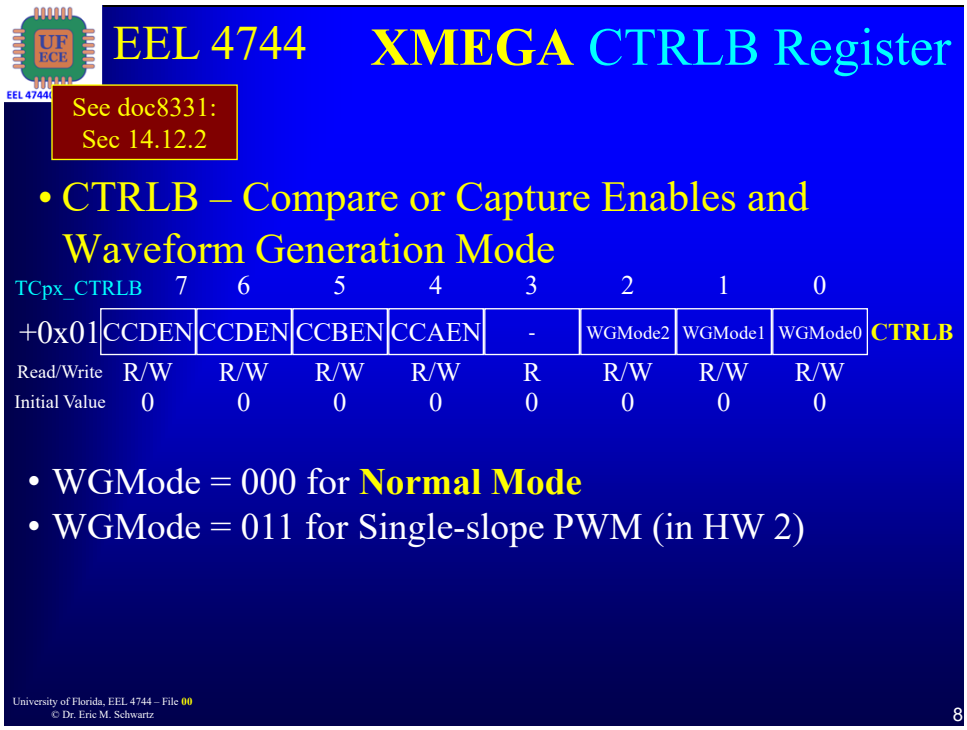
EEL 4744 XMEGA CTRLB Register
See doc8331: Sec 14.12.2
• CTRLB – Compare or Capture Enables and Waveform Generation Mode
TCpx_CTRLB 7 6 5 4 3 2 1 0
+0x01 CCDEN CCDEN CCBEN CCAEN - WGMode2 WGMode1 WGMode0 CTRLB
Read/Write R/W R/W R/W R/W R R/W R/W R/W
Initial Value 0 0 0 0 0 0 0 0
• WGMode = 000 for Normal Mode
• WGMode = 011 for Single-slope PWM (in HW 2)
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EEL 4744 **XMEGA** CTRLA & CTRLB Register

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• CTRLB WGMode Settings

See doc8331: Sec 14.12.2

WGMode [2..0]	Group Config	Mode of Operation	Top	Update	OVIF/EVENT
000	**Normal**	**Normal**	**PER**	**TOP**	**TOP**
001	FRQ	Frequency	CCA	TOP	TOP
010		Reserved	-	-	-
011	SingleSlope	Single-Slope PWM	PER	BOTTOM	BOTTOM
100		Reserved	-	-	-
101	DSTOP	Dual-Slope PWM	PER	BOTTOM	TOP
110	DSBOTH	Dual-Slope PWM	PER	BOTTOM	TOP+BOTTOM
111	DSBOTTOM	Dual-Slope PWM	PER	BOTTOM	BOTTOM

TCpx_CTRLB

	7	6	5	4	3	2	1	0
+0x01	CCDEN	CCCEN	CCBEN	CCAEN	-	WGMode2	WGMode1	WGMode0
Read/Write	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

• Example (single-slope PWM w/ CCA-CCC): TCD0_CTRLB = 0x73

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EEL 4744 **XMEGA** Interrupt Control Registers INTCTRLA & INCCTRLB

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• INTCTRLA – Enables Timer Error and Timer Overflow/Underflow interrupts as well as intr levels

TCpx_INTCTRLA

	7	6	5	4	3	2	1	0 INTCTRLA
+0x06	-	-	-	-	ERRINTLVL1	ERRINTLVL0	OVFINTLVL1	OVFINTLVL0
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

> OVFINTLVL1:0 = 00 (off); 01 (low); 10 (medium); 11 (high)

• INTCTRLB – Enables Interrupts per CC channel as well as interrupt levels

TCpx_INTCTRLB

	7	6	5	4	3	2	1	0 INTCTRLB
+0x07	CCDINTLVL1	CCDINTLVL0	CCCINTLVL1	CCCINTLVL0	CCBINTLVL1	CCBINTLVL0	CCAINTLVL1	CCAINTLVL0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

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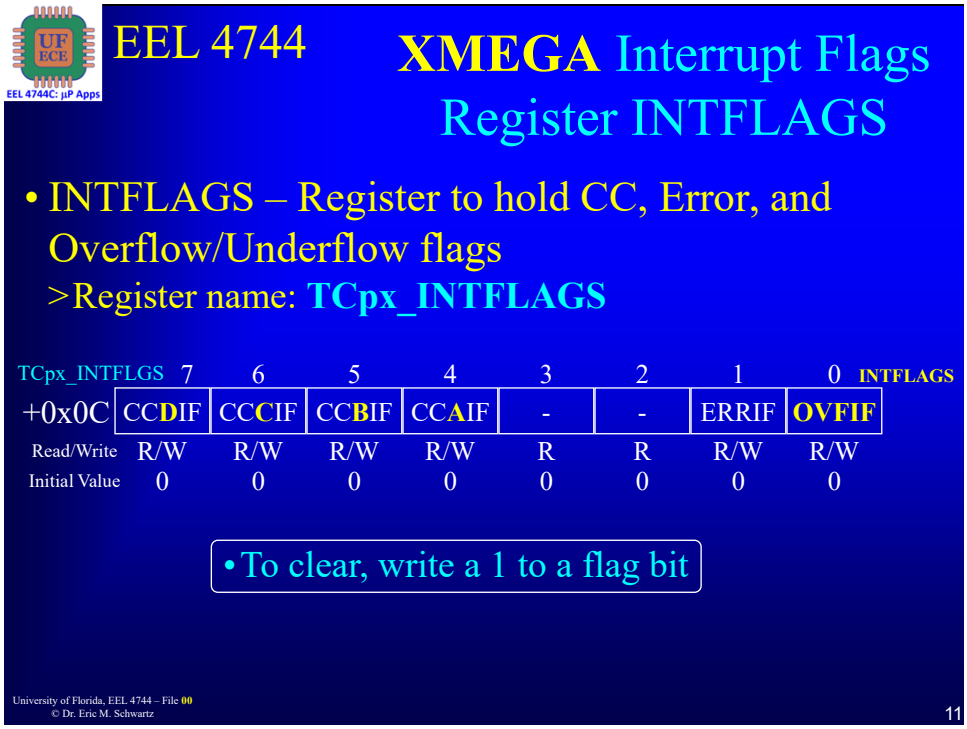
EEL 4744
XMEGA Interrupt Flags Register INTFLAGS
• INTFLAGS – Register to hold CC, Error, and Overflow/Underflow flags
>Register name: TCpx_INTFLAGS
TCpx_INTFLGS 7 6 5 4 3 2 1 0 INTFLAGS
+0x0C CCDIF CCCIF CCBIF CCAIF - - ERRIF OVFIF
Read/Write R/W R/W R/W R/W R R R/W R/W
Initial Value 0 0 0 0 0 0 0 0
• To clear, write a 1 to a flag bit
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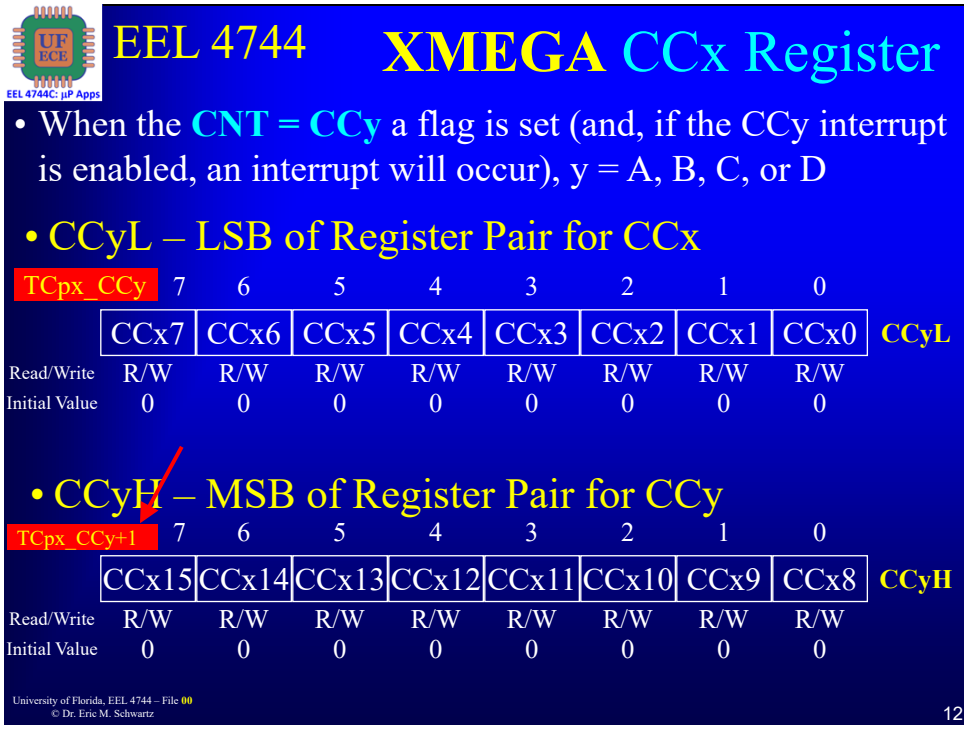
EEL 4744
XMEGA CCx Register
• When the CNT = CCy a flag is set (and, if the CCy interrupt is enabled, an interrupt will occur), y = A, B, C, or D
• CCyL – LSB of Register Pair for CCx
TCpx_CCy 7 6 5 4 3 2 1 0
CCx7 CCx6 CCx5 CCx4 CCx3 CCx2 CCx1 CCx0 CCyL
Read/Write R/W R/W R/W R/W R/W R/W R/W R/W
Initial Value 0 0 0 0 0 0 0 0
• CCyH – MSB of Register Pair for CCy
TCpx_CCy+1 7 6 5 4 3 2 1 0
CCx15 CCx14 CCx13 CCx12 CCx11 CCx10 CCx9 CCx8 CCyH
Read/Write R/W R/W R/W R/W R/W R/W R/W R/W
Initial Value 0 0 0 0 0 0 0 0
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